IN THE CLAIMS

Please cancel claims 2, 5 and 7-10 without prejudice, amend claims 1, 3-4 and 6, and add claims 11-30 as follows:

1. (Currently amended) A coding device comprising:

a coding circuit configured to generate a coded output from a digital input;

an interleaving circuit configured to generate a plurality of interleaved words; and

a rate matching circuit for adjusting the number of bits in a data block~~, the data block~~ comprising ~~a~~ said plurality of interleaved words ~~generated by the action of an interleaving circuit on a coded output generated by the action of a coding circuit on a digital input~~, the coded output having a greater number of bits than the digital input, the rate matching circuit having means for adjusting the number of bits in the data block using a rate matching pattern to provide data bits for transmission during respective frames of a transmission channel, ~~characterised in that~~ and means ~~are provided~~ for selecting the rate matching pattern depending on ~~the characteristics of the coding circuit and of the interleaving circuit~~ a bit deletion/repetition rate, wherein a bit deletion/repetition pattern is selected to ensure that the

deleted or repeated bits are not required to enable all bits from the digital input to be reconstructed.

2. (Canceled)

3.(Currently amended) A ~~rate matching circuit~~ coding device as claimed in claim 1 ~~or 2, characterised in that~~, wherein the rate matching pattern for each interleaved word within the data block is offset with respect to the adjacent interleaved word or words within the block.

4.(Currently amended) A ~~rate matching circuit~~ coding device as claimed in ~~any one of~~ claim~~s~~ 1 ~~to 3, characterised in that~~, wherein the rate matching pattern is selected as a function of the interleaving depth of the interleaving circuit.

5. (Canceled)

6.(Original) A decoding device ~~comprising~~ for decoding a signal coded by a coding device ~~as claimed in claim 5~~ having a rate matching circuit for adjusting the number of bits in a data block, the data block comprising a plurality of interleaved words

generated by the action of an interleaving circuit on a coded output generated by the action of a coding circuit on a digital input, the coded output having a greater number of bits than the digital input, the rate matching circuit having means for adjusting the number of bits in the data block using a rate matching pattern to provide data bits for transmission during respective frames of a transmission channel, and means for selecting the rate matching pattern depending on a bit deletion/repetition rate, wherein a bit deletion/repetition pattern is selected to ensure that the deleted or repeated bits are not required to enable all bits from the digital input to be reconstructed, ~~and~~ said decoding device comprising a data reconstruction circuit for reconstructing the interleaved words, a de-interleaving circuit and a channel decoder.

Claims 7-10. (Canceled)

11.(New) The coding device of claim 1, wherein the rate matching pattern forms a matrix including change bits that indicate change of corresponding bits of said interleaved words within said data block, wherein each row of said matrix includes a maximum of one of said change bits.

12. (New) The coding device of claim 1, wherein said coding circuit has one of a fixed code rate and a predetermined number of rates for a variable data source.

13. (New) The coding device of claim 1, wherein said interleaving circuit is not adaptive.

14. (New) The coding device of claim 1, wherein said interleaving circuit has a constant bit rate.

15. (New) The coding device of claim 1, wherein said coding circuit has one of a fixed code rate and a predetermined number of rates for a variable data source, and wherein said interleaving circuit is not adaptive.

16. (New) The coding device of claim 1, wherein said rate matching circuit alters a coding rate of said coding circuit.

17. (New) A decoding device for decoding a coded digital signal comprising a received data block including interleaved words, said received data block having been processed by a rate matching circuit using a rate matching pattern to adjust a number

of bits in said received data block, the decoding device comprising:

a data reconstruction circuit having means for adjusting the number of bits in said received data block to reverse action of said rate matching circuit, thereby reconstructing said interleaved words;

a de-interleaving circuit having means for generating each of said interleaved words; and

a channel decoder which receives said interleaved words provided by said de-interleaving circuit;

wherein said rate matching pattern is selected as a function of a bit deletion/repetition rate, a bit deletion/repetition pattern having been selected to ensure that the deleted or repeated bits are not required to enable all bits from the digital input to be reconstructed.

18. (New) The decoding device of claim 17, wherein change bits of said rate matching pattern for deleting or repeating bits of said data block are offset with respect to the each other along adjacent rows or columns of a matrix of said rate matching pattern.

19. (New) A method of decoding a coded digital signal comprising a received data block including interleaved words, said received data block having been processed by a rate matching circuit using a rate matching pattern to adjust a number of bits in said received data block, the method comprising:

adjusting the number of bits in said received data block to reverse action of said rate matching circuit, thereby reconstructing said interleaved words;

generating each of said interleaved words; and

receiving said interleaved words;

wherein said rate matching pattern is selected as a function of a bit deletion/repetition rate, a bit deletion/repetition pattern having been selected to ensure that the deleted or repeated bits are not required to enable all bits from the digital input to be reconstructed.

20. (New) The method of claim 19, wherein change bits of said rate matching pattern for deleting or repeating bits of said received data block are offset with respect to the each other.

21. (New) The method of claim 19, wherein change bits of said rate matching pattern for deleting or repeating bits of said

received data block are offset with respect to the each other along adjacent columns of a matrix of said rate matching pattern.

22. (New) The method of claim 19, wherein change bits of said rate matching pattern for deleting or repeating bits of said received data block are offset with respect to the each other along adjacent rows of a matrix of said rate matching pattern.

23. (New) The method of claim 19, wherein change bits of said rate matching pattern for deleting or repeating bits of said received data block are offset with respect to the each other along adjacent rows and columns of said rate matching pattern.

24. (New) The method of claim 19, wherein said received data block are formed by filling a matrix row by row with row bits of said coded output and outputs column bits of said matrix column by column to form said interleaved words.

25. (New) A method of coding a digital signal comprising:

generating a coded output from said digital signal;

generate a plurality of interleaved words from said coded output; and

adjusting the number of bits in a data block comprising said plurality of interleaved words using a rate matching pattern to provide data bits for transmission during respective frames of a transmission channel; and

selecting the rate matching pattern depending on a bit deletion/repetition rate, wherein a bit deletion/repetition pattern is selected to ensure that the deleted or repeated bits are not required to enable all bits from the digital input to be reconstructed.

26. (New) The method of claim 25, wherein change bits of said rate matching pattern for deleting or repeating bits of said data block are offset with respect to the each other.

27. (New) The method of claim 25, wherein change bits of said rate matching pattern for deleting or repeating bits of said data block are offset with respect to the each other along adjacent columns of a matrix of said rate matching pattern.

28. (New) The method of claim 25, wherein change bits of said rate matching pattern for deleting or repeating bits of said data

block are offset with respect to the each other along adjacent rows of a matrix of said rate matching pattern.

29. (New) The method of claim 25, wherein change bits of said rate matching pattern for deleting or repeating bits of said data block are offset with respect to the each other along adjacent rows and columns of said rate matching pattern.

30. (New) The method of claïm 25, wherein said data block are formed by filling a matrix row by row with row bits of said coded output and outputs column bits of said matrix column by column to form said interleaved words.